REMARKS

1. The telephone election of Claims 1-17 is hereby affirmed.

2. Claims 1-17 were rejected under 35 U.S.C. 102(b) over Yaegashi et al., U.S. patent no. 6,265,739.

Claim 1 is supported by the original disclosure as follows:

> (b) forming a first layer **(140)** ... to provide (i) the select gate **(Fig. 14A)**..., and (ii) a gate for the first peripheral transistor **(Fig. 27B)**...;
>
> (c) after forming the first layer, forming one or more second layers **(160, 170)** which provide the floating gates ....

Claim 1, and the remaining claims, are not limited to the embodiments discussed herein.

In Yaegashi's Fig. 1, the first polysilicon layer 106 is used to form both the floating gates (column 8, line 7) and the select and peripheral transistor gates (column 8, lines 40-41). Yaegashi thus does not teach or suggest forming the floating gate layer after the select or peripheral transistor gate layer. Moreover, Yaegashi teaches away therefrom because Yaegashi teaches that forming the peripheral transistor gates from the floating gate layer facilitates manufacture of high speed peripheral transistors with "a salicide structure or polymetal gates" (column 10, lines 8-15). Yaegashi also teaches in column 13, lines 48-52 that the peripheral transistor gates can be formed after the memory cell, and thus further teaches away from forming the floating gate layer after a peripheral transistor gate layer as in Applicant's Claim 1.

Claims 2-17 depend from Claim 1. Further, Claim 7 recites that the floating gate dielectric that separates the floating gates from the substrate is formed after the first layer. Claim 7 is supported by Fig. 14A, 16, showing that the floating gate dielectric ("tunnel oxide") 150 is formed on substrate 120 after select gate layer 140. See Applicant's specification, page 9, lines 16-17. Claim 7 is not limited to the embodiments discussed herein.

Yaegashi does not teach or suggest forming his memory cell gate insulating film 105 (Fig. 1) after the select gate polysilicon 106. Moreover, since the film 105 is formed before the floating gates, and the floating gates are formed from the same layer 106, Yaegashi teaches away from forming the insulation 105 after the layer 106 as recited in Claim 7.

New Claims 30-38 depend from Claim 1. Claim 30 is supported by Figs. 25, 26A, which illustrate patterning the layers 160, 170 to provide the floating and control gates.

Claim 31 is supported by Figs. 14A, 14B (patterning the layer 140 to provide the select gates while the periphery is covered by resist 820), Figs. 25, 26A (patterning the layers 160, 170 to provide the floating and control gates), and Fig. 27B and page 12, paragraph 0073 (patterning the layer 140 to provide peripheral transistor gates).

Claim 32 is supported like Claim 7 (discussed above).

Claim 33 is supported by Figs. 14A, 14B (patterning the layer 140 to provide the select gates while the periphery is covered by resist 820), Fig. 16 (forming floating gate dielectric 150 on substrate 120), and Fig. 27B and page 12, paragraph 0073 (patterning the layer 140 to provide peripheral transistor gates).

Claims 34-38 are supported by Fig. 29A, page 4, lines 25-27, page 16, paragraph 0091, pages 1-2, paragraph 0006.

Any questions regarding this case can be addressed to the undersigned at the telephone number below.

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